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For	: PRINTED WIRING BOARD AND METHOD FOR MANUFACTURING THE SAME

VERIFICATION OF TRANSLATION

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declares:

(1) that I know well both the Japanese and English languages;

(2) that I have translated the Japanese Patent Application No. 8-357959 from Japanese to English;

(3) that the attached English translation is a true and correct translation of the Japanese Patent Application No. 8-357959 to the best of my knowledge and belief; and

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MULTILAYER PRINTED CIRCUIT BOARD AND METHOD OF PRODUCING THE SAME

[Scope of Claims for Patent]

[Claim 1]
A multilayer printed circuit board comprising a substrate provided with a lower layer conductor circuit, an interlaminar insulating layer formed thereon and an upper layer conductor circuit formed on the interlaminar insulating layer, and a viahole connecting both the conductor circuits to each other, wherein
the viahole is comprised of an electroless plated film and an electrolytic plated film, and
a roughened layer is formed on at least a part of the surface of the lower layer conductor circuit connected to the viahole.

[Claim 2]
A multilayer printed circuit board according to claim 1, wherein the roughened layer is formed by the plating of copper-nickel-phosphorus alloy.

[Claim 3]
A method of producing a multilayer printed circuit board comprising steps of forming a lower layer conductor circuit on the surface of a substrate, applying a roughening treatment to at least a part of the surface of the lower conductor circuit connected to a viahole, then forming an interlaminar insulating layer on the substrate, forming openings for viaholes in the interlaminar insulating layer,
further subjecting the interlaminar insulating layer to an electroless plating, forming a plating resist thereon, subjecting the substrate to an electrolytic plating, removing the plating resist, and forming an upper layer conductor circuit comprised of the electroless plated film, the electrolytic plated film and viaholes by an etching treatment.

[Claim 4]
A method of producing a multilayer printed circuit board according to claim 3, wherein the roughened layer is formed by the plating of copper-nickel-phosphorus alloy.

[Detailed Explanation of the Invention]
[0001]
[Technical Field where the Invention belongs to]

This invention relates to a multilayer printed circuit board and a method of producing the same, and more particularly to a multilayer printed circuit board which can control the occurrence of cracks in the heat cycle without degradation of peel strength, and a method of producing the same.

[0002]

[Prior Art]

Recently, the so-called build-up multilayer wiring boards are in demand for high densification of multilayer wiring boards. This build-up multilayer wiring board is produced, for example, by a method as described in JP-B-4-55555. That is, an insulating agent composed of a photosensitive adhesive for electroless plating is applied onto a core substrate, dried, exposed to a light and developed to form an interlaminar insulating layer having openings for viaholes, and then the surface of the interlaminar insulating layer is roughened by treating with an oxidizing agent or the like, and a plating resist is formed on the roughened surface, and thereafter a non-forming portion of the plating resist is subjected to an electroless plating to form viaholes and conductor circuits, and then such steps are repeated plural times to obtain a build-up multilayer wiring board.

[0003]

[Problem to be solved by the Invention]

However, in the obtained multilayer printed circuit board, the conductor circuit is formed on the non-forming portion of the plating resist and the plating resist remains in the inner layer as it is.

If IC chips and the like are mounted on such a wiring board, warping of the board is caused by a difference of thermal expansion coefficient between the IC chip and the insulating resin layer in the heat cycle to concentrate stress into a boundary portion between the plating resist and the conductor circuit due to poor adhesion therebetween and hence cracks are generated in the interlaminar insulating layer contacting with the boundary portion.

[0004]

In order to solve such a problem, there is a method of removing the plating resist and thereafter forming a roughened layer on the surface of the conductor circuit.

For example, according to a technique described in JP-A-6-283860, there is disclosed the technique of removing the plating resist in the inner layer and providing a roughened layer of copper-nickel-phosphorus on the surface of the conductor circuit composed of an electroless plated film to prevent interlaminar peeling.

However, there is found the case of generating cracks in the interlaminar insulating resin layer contacting with viaholes, and there is required a method of controlling cracks at a portion contacting with viaholes.

[0005]

Moreover, even in the case of controlling such cracks, it is necessary to secure connection between the lower layer conductor circuit and the viahole.

It is an object of the invention to prevent cracks of the interlaminar insulating layer in the heat cycle by maintaining the other properties, particularly adhesion of the viahole to the lower layer conductor circuit.

[0006]

[Means for solving the Problem]

The point and construction of the invention are as follows.

① A multilayer printed circuit board comprising a substrate provided with a lower layer conductor circuit, an interlaminar insulating layer formed thereon and an upper layer conductor circuit formed on the interlaminar insulating layer, and a viahole connecting both the conductor circuits to each other, in which

the viahole is comprised of an electroless plated film and an electrolytic plated film, and

a roughened layer is formed on at least a part of the surface of the lower layer conductor circuit connected to the viahole.

② The roughened layer is formed by the plating of copper-nickel-phosphorus alloy.

③ A method of producing a multilayer printed circuit board comprising steps of forming a lower layer conductor circuit on the surface of a substrate, applying a roughening treatment to at least a part of the surface of the lower conductor circuit connected to a viahole, then forming an interlaminar insulating layer on the substrate, forming openings for viaholes in the interlaminar insulating layer,

further subjecting the interlaminar insulating layer to an electroless plating, forming a plating resist thereon, subjecting the substrate to an electrolytic plating, removing the plating resist, and forming an upper layer conductor circuit comprised of the electroless plated film and the electrolytic plated film and viaholes by an etching treatment.

④ The roughened layer is formed by the plating of copper-nickel-phosphorus alloy.

[0007]

The viahole is comprised of an electrolytic plated film and an electroless plated film, and the electroless plated film is located at an inner layer side and the electrolytic plated film is located at an outer layer side (see enlarged views of Fig. 18 and Fig. 19). Since the electrolytic plated film is softer and more malleable than the electroless plated film, the viahole is able to follow size change of the interlaminar insulating resin layer even if a warp of the substrate is generated in the heat cycle, and since the inner layer

side of the viahole is formed with a harder electroless plated film, and this electroless plated film is adhered to the lower layer conductor circuit through the roughened layer, peeling from the lower layer conductor circuit never occurs in the heat cycle.

[0008]

Moreover, the metal layer encroached by the roughened layer should be harder. Because the breakage at the metal layer is rarely caused even when peeling force is applied.

When the viahole is comprised of only the electrolytic plated film, even if it is adhered to the lower layer conductor circuit through the roughened layer, the electrolytic plated film itself is soft and is apt to peel off due to the heat cycle. Moreover, when the viahole is comprised of only the electroless plated film, it cannot follow the size change of the interlaminar insulating resin layer and hence the crack is caused in the interlaminar insulating resin layer existing on the viahole.

[0009]

Thus, the viahole is comprised of the electrolytic plated film and the electroless plated film in the invention, the viahole is connected to the lower layer conductor circuit through the roughened layer, so that the occurrence of cracks generated in the interlaminar insulating resin layer on the viahole and the peeling between the viahole and the lower layer conductor circuit in the heat cycle can be prevented at the same time.

In the invention, the roughened layer may be formed on the surface of the viahole. Because the roughened layer is strongly adhered to the interlaminar insulating resin layer and hence the viahole is more able to follow size change of the interlaminar insulating resin layer.

[0010]

Therefore, even when IC chips are mounted and the heat cycle test is carried out at -55℃~125℃, the occurrence of cracks is controlled and no peeling is observed.

[0011]

It is desirable that the lower layer conductor circuit connecting to the viahole is comprised of the electrolytic plated film and the electroless plated film. Moreover, the electroless plated film is located at a more inner layer side and the electrolytic plated film is located at a more outer layer side.

Since the inner layer side of the lower layer conductor circuit is adhered to the interlaminar insulating resin layer, a harder electroless plated film is desirable in order to ensure peel strength, while the opposite side is connected to the viahole, so that it is desirable to provide an electrolytic plated film having an excellent following property to size change.

Moreover, when the interlaminar insulating resin layer is roughened, it is desirable that a plated film encroached into the roughed layer is hard. Because the breakage is rarely caused at the

plated film portion when peeling force is applied.

[0012]

The roughened surface in the invention may be formed on not only the portion connecting to the viahole but also the whole surface of the lower layer conductor circuit. Because the roughened layer is excellent in adhesion to the interlaminar insulating resin layer.

The roughened layer in the invention is desirably a roughened face of copper formed by an etching treatment, a polishing treatment, an oxidation treatment and a redox treatment or a roughened face formed by a plate coating.

Particularly, the roughened layer is desirably an alloy layer of copper-nickel-phosphorus.

[0013]

The composition of the alloy layer is desirable to be 90~96 wt% of copper, 1~5 wt% of nickel and 0.5~2 wt% of phosphorus. Because, the needle-shaped structure is obtained in such a composition ratio.

[0014]

Moreover, a composition of Cu-Ni-P capable of forming the needle-shaped crystal is shown in a triangular diagram (Fig. 18). The range surrounded by (Cu, Ni, P)=(100, 0, 0), (90, 10, 0), (90, 0, 10) is preferable.

[0015]

The oxidation treatment is desirably a solution of an oxidizing agent comprising sodium chlorite, sodium hydroxide and sodium phosphate.

Furthermore, the redox treatment is carried out by immersing in a solution of sodium hydroxide and sodium borohydride after the above oxidation treatment.

[0016]

The roughened layer preferably has a thickness of 1~5 μm. If the thickness is too thick, the roughened layer itself is apt to be damaged and peeled, while if it is too thin, the adhesion property lowers.

[0017]

A thickness of the electroless plated film is preferably 1~5 μm. If the thickness is too thick, the following property to the interlaminar insulating resin layer lowers, while if it is too thin, the degradation of peel strength is caused and the electric resistance becomes large in case of being subjected to an electrolytic plating to cause the scattering in the thickness of the plated film.

[0018]

Furthermore, a thickness of the electrolytic plated film may preferably be 10~20 μm. If the thickness is to thick, the degradation of peel strength is caused, while if it is too thin, the ability to follow the interlaminar insulating resin layer lowers.

[0019]

In the invention, it is desirable to form a roughened layer on at least a side face. Because cracks generated in the interlaminar insulating resin layer due to the heat cycle result from the bad adhesion between the side face of the conductor circuit and the insulating resin layer.

[0020]

In the invention, it is desirable that the adhesive for electroless plating is used as the interlaminar insulating resin layer constituting the above wiring substrate. The adhesive for electroless plating is optimum to be obtained by dispersing cured heat-resistant resin particles soluble in an acid or oxidizing agent into an uncured heat-resistant resin hardly soluble in an acid or oxidizing agent through curing.

The heat-resistant resin particles can be dissolved and removed by treating with an acid or an oxidizing agent to form a roughened surface of octopus-trap shaped anchors on its surface.

[0021]

In the adhesive for electroless plating, the cured heat-resistant resin particles are desirable to be selected from ① heat-resistant resin powder having an average particle size of not more than 10 μm, ② aggregated particles formed by aggregating heat-resistant resin powder having an average particle size of not more than 2 μm, ③ a mixture of heat-resistant resin powder having an average particle size of not more than 10 μm and heat-resistant resin powder having an average particle size of not more than 2 μm, and ④ false particles formed by adhering at least one of heat-resistant resin powder and inorganic powder having an average particle size of not more than 2 μm onto the surface of heat-resistant resin powder having an average particle size of 2~10 μm. Because, they can form more complicated anchor.

[0022]

Next, a method of producing the printed circuit board according to the invention will be explained.

(1) At first, a wiring substrate is prepared by forming an inner layer copper pattern on the surface of a core substrate..

The copper pattern of the wiring substrate is formed by a method of etching a copper-clad laminate, or a method of forming an adhesive layer for electroless plating on a substrate such as glass epoxy substrate, polyimide substrate, ceramic substrate, metal substrate or the like and roughening the surface of the adhesive layer and subjecting the roughened surface to an electroless plating, or electroless plating the whole surface, forming a plating resist, removing the plating resist after electrolytic plating, etching treating and forming a conductor circuit comprised of an electrolytic plated film and an electroless plated film.

[0023]

Moreover, a roughened layer of copper-nickel-phosphorus is formed on the surface of the lower layer conductor circuit of the wiring substrate.

The roughened layer is formed by an electroless etching. The composition of the plating aqueous solution is desirable to have a copper ion concentration of 2.2×10^{-2}~4.1×10^{-2} mol/l, a nickel ion concentration of 2.2×10^{-3}~4.1×10^{-3} mol/l and a hypophosphorus acid ion concentration of 0.20~0.25 mol/l, respectively.

The film deposited within the above range is needle in the crystal structure, so that it is excellent in the anchor effect. The electroless plating bath may be added with a complexing agent and additives in addition to the above compounds.

[0024]

As the other method of forming the roughened layer, there are an oxidation-reduction treatment, a method of etching the copper surface along grain boundary to form a roughened layer and the like.

Moreover, through-holes are formed in the core substrate, and the front and back wiring layers may electrically be connected to each other through the through-holes.

And also, a resin may be filled in the through-holes and between the conductor circuits of the core substrate to ensure the smoothness thereof (Figs. 1~4).

[0025]

(2) Then, an interlaminar insulating resin layer is formed on the printed wiring substrate prepared in step (1). In the invention, it is particularly desirable to use an adhesive for electroless plating as an interlaminar insulating resin material (Fig. 5).

[0026]

(3) After the formed adhesive layer for electroless plating is formed, an opening portion for the formation of viahole is formed, if necessary. The opening portion for the formation of viahole is formed in the adhesive layer by light exposure, development and thermosetting in case of the photosensitive resin, or, by thermosetting and laser working in case of the thermosetting resin (Fig. 6).

[0027]

(4) Then, epoxy resin particles existing on the surface of the cured adhesive layer are dissolved and removed with an acid or an oxidizing agent to remove the surface of the adhesive layer (Fig. 7).

Here, as the acid, there are phosphoric acid, hydrochloric acid, sulfuric acid, and an organic acid such as formic acid, acetic acid or the like, particularly, the use of the organic acid is desirable. Because when it hardly corrodes the metal conductor layer exposed from the viahole by the roughening treatment.

On the other hand, as the oxidizing agent, it is desirable to use chromic acid, permanganese (potassium permanganese or

the like) and so on.
[0028]
(5) Then, a catalyst nucleus is applied to the wiring substrate provided with the roughened surface of the adhesive layer.

In the application of the catalyst nucleus, it is desirable to use a noble metal ion, a noble metal colloid or the like, and in general, palladium chloride or palladium colloid is used. Moreover, it is desirable to conduct a heating treatment for fixing the catalyst nucleus. As the catalyst nucleus, palladium is favorable.
[0029]
(6) Then, the surface of the adhesive layer for electroless plating is subjected to an electroless plating to form an electroless plated film on the whole of the roughened surface (Fig. 8). In this case, the thickness of the electroless plated film is 1~5 μm, more preferably 2~3 μm.

Then, a plating resist is formed on the electroless plated film (Fig. 9).

As the plating resist, it is particularly desirable to use a composition comprised of an imidazole curing agent and an acrylate of cresol epoxy resin, phenol novolac epoxy resin or the like, but use may be made of commercially available products.
[0030]
(7) Then, a portion not forming the plating resist is subjected to an electrolytic plating to form conductor circuits and viaholes (Fig. 10).

In this case, as the electroless plating, it is desirable to use a copper plating.
[0031]
(8) Moreover, after the plating resist is removed, the electroless plated film is removed by dissolving in an etching solution such as a mixture of sulfuric acid and hydrogen peroxide, sodium persulfate, ammonium persulfate or the like to obtain an independent conductor circuit (Fig. 11).
[0032]
(9) Then, a roughened layer is formed on the surface of the conduct circuit (Fig. 12). As the method of forming the roughened layer, there are etching treatment, polishing treatment, redox treatment and plating treatment. The redox treatment is conducted by using an oxidation aqueous solution (blackening bath) of NaOH (10 g/l), $NaClO_2$ (40 g/l) and Na_3PO_4 (6 g/l) and a reduction aqueous solution of NaOH (10 g/l) and $NaBH_4$ (5 g/l).

Furthermore, the roughened layer made from copper-nickel-phosphorus alloy layer is formed by deposition through electroless plating.
[0033]

As the electroless plating aqueous solution, it is desirable to use a plating bath of aqueous solution composition comprising copper sulfate: 1~40 g/l, nickel sulfate: 0.1~6.0 g/l, citric acid:

10~10 g/l, hypophosphite: 10~100 g/l, boric acid: 10~40 g/l and surfactant: 0.01~10 g/l.

[0034]

(10) The adhesive layer for electroless plating as an interlaminar insulating resin layer is formed on the substrate (Fig. 13).

(11) Moreover, an upper layer conductor circuit is formed by repeating steps (3) ~ (8) (Figs. 14~17).

[0035]

(12) Then, the coating film of the solder resist composition is dried, and a photomask film depicted with an opening portion is placed on the dried film, which is subjected to light exposure and developing treatments to form an opening portion exposing a pad portion of the conductor circuit. Here, the opening size of the opening portion may be made larger than the diameter of the pad to completely expose the pad.

[0036]

(11) Then, a metal layer of "nickel-gold" is formed on the pad portion exposed from the opening portion.

[0037]

(12) Then, a solder body is fed onto the pad portion exposed from the opening portion.

As a method of feeding the solder body, use may be made of a solder transferring method and a solder printing method. Here, the solder transferring method is a method wherein a solder foil is attached to a prepreg and etched to as to leave only a portion corresponding to the opening portion to render into a solder carrier having a solder pattern, and the solder carrier film is laminated so as to contact the solder pattern with the pad after a flux is applied to the opening portion in the solder resist of the substrate and heated to transfer the solder onto the pad. On the other hand, the solder printing method is a method wherein a metal mask having through-holes corresponding to the pads is placed onto the substrate and a solder paste is printed and heated.

[0038]

[Example]

(Example 1)

(1) As a starting material, there is used a copper-clad laminate obtained by laminating a copper foil of 18 μm on both faces of a substrate 1 made from a glass epoxy resin or BT (bismaleimide triazine) resin having a thickness of 0.6 mm. The copper foil of the copper-clad laminate is etched in a pattern according to the usual manner, which is pierced and subjected to an electroless plating to form a lower layer conductor circuit 2 and through-holes on both faces of the substrate.

Further, bisphenol F- epoxy resin is filled between the conductor circuit and in the through-holes.

[0039]

(2) The substrate formed with the inner layer copper pattern in step (1) washed with water, dried, acidicly degreased and soft-etched, then, treated with a catalyst solution comprising palladium chloride and organic acid to give a Pd catalyst, which is activated and subjected to a plating in an electroless plating bath comprising 8 g/l of copper sulfate, 0.6 g/l of nickel sulfate, 15 g/l of citric acid, 29 g/l of sodium hypophosphate, 31 g/l of boric acid and 0.1 g/l of a surfactant and having pH=9 to form a roughened layer 5 (uneven layer) of Cu-Ni-P alloy having a thickness of 2.5 μm on the whole surface of the copper conductor circuit.

[0040]

(3) A photosensitive adhesive solution (interlaminar resin insulating agent) is prepared by mixing 70 parts by weight of 25% acrylated product of cresol novolac epoxy resin (made by Nippon Kayaku Co., Ltd., molecular weight: 2500) dissolved in DMDG (diethylene glycol dimethyl ether), 30 parts by weight of polyether sulphone (PES), 4 parts by weight of an imidazole curing agent (made by Shikoku Kasei Co., Ltd., trade name: 2E4MZ-CN), 10 parts by weight of caprolacton-modified tris(acroxyethyl) isocyanurate (made by Toa Gosei Co., Ltd., trade name: Aronix M325) as a photosensitive monomer, 5 parts by weight of benzophenone (made by Kanto Kagaku Co., Ltd.) as a photoinitiator, 0.5 part by weight of Micheler's ketone (made by Kanto Kagaku Co., Ltd.) as a photosensitizer and 35 parts by weight at 5.5 μm on average and 5 parts by weight at 0.5 μm on average of epoxy resin particles, adding NMP (normal methyl pyrolidone), adjusting a viscosity to 12 Pa·s in a homodisperser agitating machine and kneading them through three rolls to obtain a photosensitive adhesive solution (interlaminar insulating resin material).

[0041]

(4) The photosensitive adhesive solution obtained in step (3) is applied onto both faces of the substrate treated in step (2) by means of a roll coater and left to stand at a horizontal state for 20 minutes and dried at 60℃ for 30 minutes to form an adhesive layer 6 of 60 μm in thickness.

(5) A photomask film depicted with viaholes is adhered onto both faces of the substrate provided with the adhesive layer 6 in step (4) and exposed by irradiation of ultraviolet rays.

[0042]

(6) The exposed substrate is developed by spraying a DMTG (triethylene glydimethylether) solution to form openings for viaholes of 100 μm ϕ in the adhesive layer. The substrate is further exposed to a superhigh pressure mercury lamp at 3000 mJ/cm^2 and then heated at 100℃ for 1 hour and at 150℃ for 5 hours to form an adhesive layer of 50 μm in thickness having the openings (openings for the formation of viaholes) with excellent

size accuracy corresponding to the photomask film. Moreover, the roughened layer is partially exposed in the opening for the viahole.

[0043]

(7) The substrate provided with the openings for the viahole in steps (5), (6) is immersed in chromic acid for 2 minutes to dissolve and remove epoxy resin particles from the surface of the adhesive layer, whereby the surface of the adhesive layer is roughened, and thereafter, it is immersed in a neutral solution (made by Shipley) and washed with water.

(8) A palladium catalyst (made by Atotec Co., Ltd.) is applied to the substrate subjected to a roughening treatment (roughening depth: 5 μm) in step (7) to give a catalyst nucleus to the surface of the adhesive layer and the opening for the viahole.

[0044]

(9) The substrate is immersed in an electroless copper plating bath having the following composition to form an electroless copper plated film 3 having a thickness of 3 μm over the full roughened surface.

Electroless plating aqueous solution

EDTA	150 g/l
Copper sulfate	20 g/l
HCHO	30 ml/l
NaOH	40 g/l
α, α'bipyridyl	80 g/l
PEG	0.1 g/l

electroless plating condition

liquid temperature for 70℃ for 30 minutes

[0045]

(10) A commercially available photosensitve dry film is attached to the electroless copper plated film and a mask is plated, exposed to a light at 100 mJ/cm^2 and developed with 0.8% sodium carbonate to form a plating resist 7 having a thickness of 15 μm.

[0046]

(11) Then, an electrolytic copper plated film 4 having a thickness of 10 μm is formed by applying an electrolytic copper plating under the following conditions.

Electrolytic plating aqueous solution

sulfuric acid	180 g/l
copper sulfate	80 g/l
additive (made of Adotec Japan,trade name: Capalacido GL)	1 ml/l

Electrolytic plating condition

current density	1 A/dm^2
temperature	room temperature

[0047]

(12) After the plating resist 7 is peeled and removed with 5% KOH, the electroless plated film 3 is dissolved and removed by etching with a mixed solution of sulfuric acid hydrogen peroxide to

form conductor circuits (including viaholes) of 18 μm in thickness comprises of the electroless copper plated film and the electrolytic copper plated film 4.

[0048]

(13) The substrate provided with the conductor circuit is immersed in an electroless plating aqueous solution comprising 8 g/l of copper sulfate, 0.6 g/l of nickel sulfate, 15 g/l of citric acid, 29 g/l of sodium hypophosphite, 31 g/l of boric acid and 0.1 g/l of surfactant and having pH=9 to form a roughened layer 5 of copper-nickel-phosphorus having a thickness of 3 μm on the surface of the conductor circuit.

When the roughened layer 5 is analyzed by EPMA (electro probe micro analyzer), it shows a composition ratio of Cu: 98 mol%, Ni: 1.5 mol% and P: 0.5 mol%.

[0049]

(14) Steps (4)~(12) are repeated to further form an upper layer conductor circuit.

[0050]

(15) On the other hand, a solder resist composition is prepared by mixing 46.67 g of photosensitized oligomer (molecular weight: 4000) in which 50% of epoxy group in 60% by weight of cresol novolac epoxy resin (made by Nippon Kayaku Co., Ltd.) dissolved in DMDG is acrylated, 15.0 g of 80% by weight of bisphenol A- epoxy resin (made by Yuka Shell Co., Ltd., trade name: Epikote 1001) dissolved in methyl ethyl ketone, 1.6 g of an imidazole curing agent (made by Shikoku Kasei Co., Ltd., trade name: 2E4MZ-CN), 3 g of a polyvalent acrylic monomer (made by Nippon Kayaku Co., Ltd, trade name: R604) as a photosensitive monomer, 1.5 g of a polyvalent acrylic monomer (made by Kyoei Kagaku Co., Ltd., trade name: DPE6A), 0.71 g of a dispersion defoaming agent (made by Sannopuko Co., Ltd., trade name: S-65), further 2 g of benzophenone (made by Kanto Kagaku Co., Ltd.) as a photoinitiator and 0.2 g of Micheler's ketone (made by Kanto Kagaku Co., Ltd.) as a photosensitizer and adjusting a viscosity to 2.0 Pa·s at 25℃.

Moreover, the measurement of the viscosity is carried out by means of a B- viscometer (made by Tokyo Keiki Co., Ltd., DVL-B model) with a rotor No. 4 in case of 60 rpm or a rotor No. 3 in case of 6 rpm.

[0051]

(16) The solder resist composition is applied onto the substrate at a thickness of 20 μm.

(17) Then, after dried at 70℃ for 20 minutes, the substrate is exposed to ultraviolet rays at 1000 mJ/cm^2 and developed with DMTG.

Furthermore, it is heated at 80℃ for 1 hour, at 100℃ for 1 hour, at 120℃ for 1 hour and 150℃ for 3 hours to form a solder

resist layer (thickness: 20 μm) opened in the pad portion (opening size: 200 μm).

[0052]

(18) Then, the substrate provided with the solder resist layer is immersed in an electroless nickel plating solution of pH=5 comprising 30 g/l of nickel chloride, 10 g/l of sodium hypophosphite and 10 g/l of sodium citrate for 20 minutes to form a nickel plated layer 13 having a thickness of 5 μm in the opening portion. Further, the substrate is immersed in an electroless gold plating solution comprising 2 g/l of potassium gold cyanide, 75 g/l of ammonium chloride, 50 g/l of sodium citrate and 10 g/l of sodium hypophosphite at 93% for 23 seconds to form a gold plated layer having a thickness of 0.03 μm on the nickel plated layer 13.

[0053]

(19) Then, a solder paste is printed on the opening portion of the solder resist layer and reflowed at 200℃ to form solder bumps, whereby there is produced a printed circuit board having solder bumps.

[0054]

(Example 2)

A printed circuit board is produced fundamentally in the same manner as in Example 1 except that the roughening is carried out by etching. An etching solution of a trade name "Durabond" made by Meck Co., Ltd. is used.

[0055]

(Comparative Example)

A dry film photoresist is laminated on the substrate treated in steps (1), (2), (3), (4), (5), (6), (7) and (8) of Example 1 exposed and developed to form a plating resist. Then, after step (9) of Example 1 is carried out, the plating resist is peeled in the same manner as in step (12) and the whole surface of the conductor circuit is roughened by step (13), thereafter, the formation of interlaminar insulating resin layer, roughening treatment, the formation of plating resist and electroless copper plating are carried out in the same manner, and after the plating resist is peeled, a printed circuit board having solder bumps is produced by carrying steps of (15), (16), (17), (18) and (19) of Example 1.

[0056]

After IC chip is mounted onto each of the printed circuit boards of Examples and Comparative Example, heat cycle tests of 1000 cycles and 2000 cycles under conditions of -55℃ for 15 minutes, room temperature for 10 minutes and 125℃ for 15 minutes are carried out.

Occurrences of cracks of the interlaminar insulating resin layer on the viahole in Examples and Comparative Example are confirmed by means of a scanning electron microscope. Furthermore, the presence or absence of the peeling between a

viahole and a lower layer conductor circuit is confirmed in the same manner.

[0057]

[Table 1]

	Occurrence of cracks		Peeling of viaholes	
	1000 cycles	2000cycles	1000 cycles	2000cycles
Example 1	None	None	None	None
Example 2	None	None	None	None
Comparative Example	None	Yes	None	Yes

[0058]

[Effect of the Invention]

As explained above, according to a printed circuit board of the invention, it is possible to simultaneously control the occurrence of cracks occurred in the interlaminar insulating resin layer on the viahole in the heat cycle and the peeling between the viahole and the lower layer conductor circuit, and as a result it is possible to improve connection reliability.

[Brief Description of the Drawings]

[Fig. 1]~[Fig. 17]

Flowcharts of a multilayer printed circuit board according to the invention.

[Fig. 18]

A structure enlarged view of a multilayer printed circuit board according to the invention.

[Fig. 19]

A structure enlarged view of a multilayer printed circuit board according to the invention.

[Fig. 20]

A triangular diagram showing the composition of a copper-nickel-phosphorus roughened layer.

[Explanation of the Signs]

1 substrate
2 lower layer conductor circuit
3 electroless copper plated film
4 electrolytic copper plated film
5 roughened layer
6 interlaminar insulating resin layer (adhesive layer for electroless plating)
7 plating resist
20 upper layer conductor circuit

[Name of the Document] Abstract
[Subject]

To control cracks of interlaminar insulating resin layer on viahole due to heat cycle and peeling between viahole and lower layer conductor circuit.

[Solution]

A viahole is comprised of an electrolytic plated film and an electroless plated film, and a portion connecting to the viahole in a lower layer conductor circuit is provided with a roughened layer.

[Selected Drawing] Fig. 18